CLAIMS

What is claimed is:

1.   A method comprising:

associating blocks of instructions between start and end of a critical section with color information, the blocks corresponding to a program trace and containing a wait instruction; and

sinking the wait instruction down the blocks globally to the end of the critical section using the color information and a dependence constraint on the wait instruction.

2.   The method of claim 1 wherein associating the blocks comprises:

identifying a sequence of the blocks corresponding to the program trace from a starting block at the start of the critical section to an ending block at the end of the critical section, the starting block containing the wait instruction; and

assigning a color to the sequence of the blocks and the wait instruction.

3.   The method of claim 1 wherein sinking the wait instruction comprises:

speculatively moving the wait instruction to a basic block having multiple predecessor blocks, the multiple predecessor blocks including the starting block;

inserting compensation code to at least one of the multiple predecessors excluding the starting block; and

updating the color information.

4.   The method of claim 3 wherein speculatively moving the wait instruction comprises:

moving the wait instruction to the basic block if the starting block and the wait instruction have same color and if the wait instruction is ready.

5.   The method of claim 3 wherein inserting the compensation code comprises:

inserting a send signal to the at least one of the multiple predecessors excluding the starting block.

6.   The method of claim 3 wherein updating the coloring information comprises:

resetting the color of the basic block; and

resetting the color of the wait instruction having an associated memory access instruction in the basic block.

7. The method of claim 6 wherein updating the color information further comprises:

changing the color of the wait instruction to intersection of reset color of the wait instruction and the reset color of the basic block.

8. A program transformer comprising:

a color associator to associate blocks of instructions between start and end of a critical section with color information, the blocks corresponding to a program trace and containing a wait instruction; and

a code mover and compensator coupled to the color associator to sink the wait instruction down the blocks globally to the end of the critical section using the color information and a dependence constraint on the wait instruction.

9. The program transformer of claim 8 wherein the color associator comprises:

a trace identifier to identify a sequence of the blocks corresponding to the program trace from a starting block at the start of the critical section to an ending block at the end of the critical section, the starting block containing the wait instruction; and

a color assigner coupled to the trace identifier to assign a block color to the sequence of the blocks and a wait color to the wait instruction.

10. The program transformer of claim 8 wherein the code mover and compensator comprises:

a code mover to speculatively move the wait instruction to a basic block having multiple predecessor blocks, the multiple predecessor blocks including the starting block;

a code compensator to insert compensation code to at least one of the multiple predecessors excluding the starting block; and

a color updater to update the color information.

11.   The program transformer of claim 10 wherein the code mover moves the wait instruction to the basic block if the block color of the starting block and the wait color of the wait instruction have same color and if the wait instruction is ready.

12.   The program transformer of claim 10 wherein the code compensator inserts a send signal to the at least one of the multiple predecessors excluding the starting block.

13.   The program transformer of claim 10 wherein the color updater resets the block color of the basic block, and the wait color of the wait instruction having an associated memory access instruction in the basic block.

14.   The program transformer of claim 10 wherein the color updater changes the wait color of the wait instruction to intersection of reset wait color of the wait instruction and the reset block color of the basic block.

15.   A system comprising:
a network processor;
a host processor coupled to the network processor; and
a memory coupled to the host processor having a program transformer to transform a program module to be executed on the network processor, the program transformer comprising:

        a color associator to associate blocks of instructions between start and end of a critical section with color information, the blocks corresponding to a program trace and containing a wait instruction, and

        a code mover and compensator coupled to the color associator to sink the wait instruction down the blocks globally to the end of the critical section using the color information and a dependence constraint on the wait instruction.

16.   The system of claim 15 wherein the color associator comprises:
a trace identifier to identify a sequence of the blocks corresponding to the program trace from a starting block at the start of the critical section to an ending block at the end of the critical section, the starting block containing the wait instruction; and

a color assigner coupled to the trace identifier to assign a block color to the sequence of the blocks and a wait color to the wait instruction.

17.   The system of claim 15 wherein the code mover and compensator comprises:

a code mover to speculatively move the wait instruction to a basic block having multiple predecessor blocks, the multiple predecessor blocks including the starting block;

a code compensator to insert compensation code to at least one of the multiple predecessors excluding the starting block; and

a color updater to update the color information.

18.   The system of claim 17 wherein the code mover moves the wait instruction to the basic block if the block color of the starting block and the wait color of the wait instruction have same color and if the wait instruction is ready.

19.   The system of claim 17 wherein the code compensator inserts a send signal to the at least one of the multiple predecessors excluding the starting block.

20.   The system of claim 17 wherein the color updater resets the block color of the basic block, and the wait color of the wait instruction having an associated memory access instruction in the basic block.

21.   The system of claim 17 wherein the color updater changes the wait color of the wait instruction to intersection of reset wait color of the wait instruction and the reset block color of the basic block.

22.   An article of manufacture comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform operations comprising:

associating blocks of instructions between start and end of a critical section with color information, the blocks corresponding to a program trace and containing a wait instruction; and

sinking the wait instruction down the blocks globally to the end of the critical section using the color information and a dependence constraint on the wait instruction.

23.   The article of manufacture of claim 22 wherein the data causing the machine to perform associating the blocks comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

identifying a sequence of the blocks corresponding to the program trace from a starting block at the start of the critical section to an ending block at the end of the critical section, the starting block containing the wait instruction; and

assigning a block color to the sequence of the blocks and a wait color to the wait instruction.

24.   The article of manufacture of claim 22 wherein the data causing the machine to perform sinking the wait instruction comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

speculatively moving the wait instruction to a basic block having multiple predecessor blocks, the multiple predecessor blocks including the starting block;

inserting compensation code to at least one of the multiple predecessors excluding the starting block; and

updating the color information.

25.   The article of manufacture of claim 24 wherein the data causing the machine to perform speculatively moving the wait instruction comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

moving the wait instruction to the basic block if the block color of the starting block and the wait color of the wait instruction have same color and if the wait instruction is ready.

26.   The article of manufacture of claim 24 wherein the data causing the machine to perform inserting the compensation code comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

inserting a send signal to the at least one of the multiple predecessors excluding the starting block.

27.   The article of manufacture of claim 24 wherein the data causing the machine to perform updating the coloring information comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

resetting the block color of the basic block; and

resetting the wait color of the wait instruction having an associated memory access instruction in the basic block.

28.   The article of manufacture of claim 27 wherein the data causing the machine to perform updating the color information further comprises data that, when accessed by a machine, cause the machine to perform operations comprising:

changing the wait color of the wait instruction to intersection of reset block color of the wait instruction and the reset block color of the basic block.